DRIVING METHOD OF DISPLAY PANEL AND DISPLAY DEVICE

FIELD OF THE INVENTION

The present invention relates to a driving method of a display panel such as a plasma display panel (PDP), a plasma addressed liquid crystal (PALC), a liquid crystal display (LCD) or a field emission display (FED), and to a thin type display device.

DESCRIPTION OF THE PRIOR ART

A display panel is used as a device replacing a CRT in various fields. For example, a PDP is commercialized as a wall-hung TV set having a large screen above 40 inches. One of challenges to high definition and a large screen is a countermeasure against capacitance between electrodes.

As shown in Fig. 16, a display panel comprises scan electrodes S_1, S_2, ..., S_N for row selection and data electrodes A_1, A_2, ..., A_M for column selection, which are arranged in a matrix. The suffix of the reference letter indicates an arrangement order of the electrode. A unit display area is defined at each of intersections of the scan electrodes S_1-S_N and the data electrodes A_1-A_M, and a display element is disposed at each of the unit display area. Fig. 16 typically shows display elements of a first row and a second row in the (m+1)th column. As shown in Figs. 17A to 17D using symbols, display elements of a PDP and a PALC are discharge cells. An LCD has liquid cells as the display elements, while an FED has field emitters as the display elements. Furthermore, a

commercialized surface discharge type PDP has two electrodes arranged for each row, and only one of the two electrodes is used for the row selection. Therefore, the electrode structure of the surface discharge type PDP is considered as a simple matrix similar to that of other types from the viewpoint of the display element selection.

Contents of display are set by line sequential addressing as shown in Fig. 18. An address period TA of one frame is divided into row selection periods Ty whose number is the same as the number of lines N of the screen. Each of the scan electrodes S_1-S_N is biased to a predetermined potential to be active in any one of the row selection periods Ty. Usually, the scan electrode is activated in order from an end of the arrangement in every row selection period. In synchronization with this row selection, display data of a row are outputted from data electrodes A_1-A_M for each row selection period. Namely, potential of all data electrodes A_1-A_M are controlled at the same time corresponding to the display data. The potential is controlled in a binary manner or in a multivalued manner for gradation display.

The binary control of the potential of the data electrodes A_1-A_M utilizes a switching circuit having a push-pull structure according to an embodiment of the present invention as shown in Fig. 5. Only one switching element Q1, constituting a pair of switching elements Q1 and Q2, is turned on so as to connect the data electrode A_m to a power supply terminal of a driving power source (a high potential terminal of a voltage output). Otherwise, only the other switching element Q2 is turned on so as to

connect the data electrode A_m to a current sink terminal of the driving power source (a ground terminal, in general). ON or OFF of each switching element Q1 or Q2 is determined by the display data D_m of the corresponding column.

Fig. 20 is a time chart for controlling the data electrode in the conventional driving method.

It is supposed that a pair of switches SW1 and SW2 control the potential of the data electrode A_m. The switch SW1 corresponds to the above-mentioned switching element Q1, and the switch SW1 corresponds to the switching element Q2.

In a push-pull structure, it must be avoided that a pair of switches SW1 and SW2 are turned on at the same time, which causes a short circuit of the driving power source. Therefore, in order to prevent the short circuit securely when the row selection is switched under the condition where the display data D_m are different between n-th ($1 \leqq n < N$) row selection and the next (n+1)th row selection, both the switches SW1 and SW2 are turned off between the row selection periods Ty. In other words, in the n-th row selection period Ty, when one of the switches SW1 and SW2 is turned on, the switch SW1 or the switch SW2 is turned on at the starting stage of the row selection period Ty and is turned off before the end point of the row selection period Ty. This operation is performed by controlling the switches SW1 and SW2 using the AND signal of the timing signal TSC turning on and off in the row selection period and the display data D_m of the corresponding m-th column.

In the conventional method, the on and off timings of the switch SW1 are the same as those of the switch SW2 for the start point of the row selection period Ty. In addition, the on and off timings of the switching element is also the same between the neighboring data electrodes. The conventional driving method had a problem in that there was much loss of power for charging a capacitance between the neighboring data electrodes. Hereinafter, this problem will be explained in detail.

It is supposed that the addressing is performed in a pattern in which potential of the data electrodes are switched oppositely between the m-th column and the neighboring (m+1)th column as shown in Fig. 20, and the potential are switched in both columns every row selection period Ty. In this pattern, the display data D_m of the m-th column and the display data D_{m+1} of the (m+1)th column are set 0 or 1 alternately. The contents of the display are as shown in Fig. 19.

Fig. 21 shows the problem of the conventional method.

The problem is that when biasing the data electrode to the polarity opposite to the charge stored between the data electrodes, current canceling the charge must be supplied as being explained below.

[Step 1] At the time point just before the end of the row selection period Ty, the switches $SW1_m$ and $SW2_m$ of the m-th column and the switches $SW1_{m+1}$ and $SW2_{m+1}$ of the (m+1)th column are off (high impedance state). The capacitance between the data electrodes is charged so that the m-th column side has the positive polarity (+) and the (m+1)th column side has the negative polarity (-). The

letters in the parentheses indicate potentials in Fig. 21.

[Step 2] At the time point when the switches $SW2_m$ and $SW1_{m+1}$ are turned on at the same time, the data electrode A_m is connected to the ground, and the potential of the data electrode A_{m+1} drops to -Va, so that current Ia canceling the charge stored in the capacitance between the data electrodes starts to flow from the power source passing through the switch $SW1_{m+1}$. This current Ia is accumulated as power consumption of the display panel. At the moment when the stored charge is cancelled (discharged) completely, the voltage between the data electrodes becomes zero volts.

[Step 3] Following the current Ia, new current Ib flows for charging the capacitance between the data electrodes to a polarity opposite to the previous polarity. This current Ib is also supplied by the power source and is accumulated as power consumption. The current Ia is equal to the current Ib in the principle.

As explained above, the conventional driving method consumes power for discharging and charging the capacitance between the data electrodes. Furthermore, there is a method for reducing the power consumption, in which a reset period is provided so that all the switches $SW2_m$ and $SW2_{m+1}$ of the current sink side are turned on. When the switches $SW2_m$ and $SW2_{m+1}$ are turned on, the data electrodes are connected via the ground side power source line, so that the stored charge is discharged. However, there are two problems in this method. One of the problems is that since a period for turning off all the switches $SW1_m$, $SW1_{m+1}$, $SW2_m$ and $SW2_{m+1}$ in the current

supplying side and the current sink side is required in order to prevent the short circuit of the power source after the reset period, the row selection period Ty is elongated due to the period, resulting in drop of the display speed. The other problem is that the potential of the data electrodes A_m and A_{m+1} are switched every row selection period Ty even if the display data D_m and D_{m+1} are constant as in the case where a line in the column direction is drawn, thereby power is consumed for charging and discharging the capacitance between the data electrodes.

An object of the present invention is to reduce undesired power consumption due to the capacitance between the data electrodes.

SUMMARY OF THE INVENTION

In the display panel to which the present invention is applied, during the period satisfying setting conditions in addressing, one of neighboring data electrodes is connected to a power source terminal, and the data electrodes are connected to each other by a short circuit of a current path including a diode provided between the other data electrode and the power source terminal and a power source line, so that charge stored in capacitance between the data electrodes is discharged.

The principle of the present invention is shown in Figs. 1 and 2. For the data electrode A_m of the m-th column that is any noted column, backward current paths P1 and P2 are formed in parallel with each of switches $SW1_m$ and $SW2_m$ controlling the potential in binary manner. The

backward current paths P1 and P2 are obtained by connecting diodes, or using switching elements having parasitic diodes as the switches $SW1_m$ and $SW2_m$. The backward means the direction in which the current supply terminal side (high potential side) of the power source is a cathode and the current sink terminal side (low potential side) is an anode. In the same way, for the data electrode A_{m+1} of the (m+1)th column too, a switching circuit having backward current paths P1 and P2 is provided.

In the addressing to which the present invention is applied, in synchronization with the row selection the data electrode A_m is switched from the bias potential (Va) to the ground potential (0), and oppositely the data electrode A_{m+1} is switched from the ground potential (0) to the bias potential (Va). This switching control has a first process called "L reset" and a second process called "H reset".

The L reset includes a step of discharging the capacitance between the data electrodes using the backward current path P2 of the current sink terminal side (ground side) as shown in Fig. 1.

[Step 1] At the tie point just before the end of the row selection period Ty, the switches $SW1_m$ and $SW2_m$ of the m-th column and the switches $SW1_{m+1}$ and $SW2_{m+1}$ of the (m+1)th column are off (high impedance state). The capacitance between the data electrodes is charged in the manner that the m-th column side is the positive polarity (+), and the (m+1)th column side is the negative polarity (-).

[Step 2] When only the switch $SW2_m$ is turned on, the potential of the data electrode A_{m+1} drops to -Va. As a result, current Ia flows from the ground line to the data electrode A_{m+1} via the backward current path P2 that is parallel with the switch $SW2_{m+1}$. At the same time, the current Ia flows from the data electrode A_m to the ground line via the switch $SW2_m$. Namely, the charge between the data electrodes is discharged by a closed loop including the ground line, and power source does not supply current.

[Step 3] The current Ia flows until the data electrode A_{m+1} becomes the ground potential (0).

[Step 4] When the switch $SW1_{m+1}$ is turned on while the switch $SW2_m$ is turned off, current Ib charging the capacitance flows from the current supply line to the data electrode A_{m+1} until the potential of the data electrode A_{m+1} rises from the ground potential to the bias potential (Va).

In the L reset, though the current Ia and the current Ib flow in the same way as the conventional method, the current Ia related to the discharge of the capacitance does not depend on the current supply from the power source. Therefore, power consumption related to the capacitance is a half of the conventional method.

H reset includes a step of discharging the capacitance between the data electrodes using the backward current path P1 of the current supply terminal side as shown in Fig. 2.

[Step 1] The switches $SW1_m$, $SW2_m$, $SW1_{m+1}$ and $SW2_{m+1}$ are off (high impedance state). The capacitance between the data electrodes is charged in the manner that the m-th

column side is positive (+), and the (m+1)th column side is negative (-).

[Step 2] When only the switch $SW1_{m+1}$ is turned on, the potential of the data electrode A_m rises from Va to 2Va. As a result, the current Ia flows from the data electrode Am to the current supply line passing through the backward current path P1 that is parallel with the switch $SW1_m$. At the same time, the current Ia flows from the current supply line to the data electrode A_{m+1} via the switch $SW2_m$. Namely, the charge between the data electrodes is discharged by a closed loop including the current supply line, and power source does not supply current.

[Step 3] The current Ia flows until the data electrode A_{m+1} becomes the bias potential (Va).

[Step 4] When the switch $SW2_m$ is turned on while the switch $SW1_{m+1}$ is turned on, the current Ib charging the capacitance between the data electrodes flows until the potential of the data electrode A_m drops to ground potential.

In the H reset, though the current Ia and the current Ib flow in the same way as the conventional method, the current Ia relating to the discharge of the capacitance does not depend on the current supply from the power source. Therefore, power consumption relating to the capacitance is a half of the conventional method.

The above-mentioned L reset and H reset are effective in the case where the switching of the display data in the neighboring data electrodes are opposite to each other as explained above. However, it is unnecessary

for controlling the switches $SW1_m$, $SW2_m$, $SW1_{m+1}$ and $SW2_{m+1}$ to decide whether the display data are different between the n-th row and the (n+1)th row in each column, or whether the display data are different between the neighboring columns. The L reset and the H reset are realized by shifting the control timing between the switch SW1 and the switch SW2 for all columns, or by shifting the control timing of the switches SW1 and SW2 between the odd column and the even column.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the principle of the present invention.

Fig. 2 is a diagram showing the principle of the present invention.

Fig. 3 is a block diagram of a main portion of a display device according to a first embodiment.

Fig. 4 is a functional block diagram of a driver according to the first embodiment.

Fig. 5 is a schematic circuit diagram of the driver according to the first embodiment.

Fig. 6 is an equivalent circuit diagram of an FET.

Fig. 7 is a time chart of data electrode control according to the first embodiment.

Fig. 8 is a time chart of the data electrode control according to the first embodiment.

Figs. 9A to 9D are diagrams each showing an example of a delay circuit.

Fig. 10 is a schematic circuit diagram of the driver according to a variation of the first embodiment.

Fig. 11 is a block diagram of a main portion of a display device according to a second embodiment.

Fig. 12 is a time chart of the data electrode control according to the second embodiment.

Fig. 13 is a block diagram of a main portion of a display device according to a third embodiment.

Fig. 14 is a block diagram of a main portion of a display device according to a fourth embodiment.

Fig. 15 is a block diagram of a main portion of a display device according to a fifth embodiment.

Fig. 16 is a schematic diagram of an electrode matrix.

Figs. 17A to 17D are diagrams each showing an example of a display element.

Fig. 18 is a time chart showing a scheme of line sequential addressing.

Fig. 19 is a diagram showing an example of a display pattern.

Fig. 20 is a time chart of data electrode control in the conventional driving method.

Fig. 21 is a diagram showing a conventional problem.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in Fig. 3, a display device 1 comprises a display panel 11 having a screen including M × N display elements and a drive unit 21 for controlling potential of scan electrodes S_1-S_N and data electrodes A_1-A_M. The drive unit 21 includes a controller 31, a power source circuit 41, a driver 51 of the scan electrodes S_1-S_N and a driver 61 of the data electrodes A_1-A_M. The driver 61 includes a

plurality of integrated circuit chips 71_1-71_k having the same structure being charged in controlling 256 data electrodes A_1-A_M, for example. The controller 31 transfers display data D_1-D_M of M columns selected in each row selection period Ty of the addressing to the driver 61 serially and gives control signals LAT, SUS and TSC that will be explained later to the driver 61.

As shown in Fig. 4, in the driver 61, a set of the integrated circuit chips 71_1-71_k constitute four functional blocks including a shift register 101, a latch circuit 111, an output control circuit 121 and an output circuit 131. The shift register 101 inputs display data D_1-D_M serially and outputs the display data D_1-D_M in parallel. The output control circuit 121 generates switching signals corresponding to combinations of the display data D1-DM latched in accordance with the signal LAT and control signals SUS, TSC and TSC'. The control signal SUS is a low-active signal for separating all data electrodes A_1-A_M as a single unit from the high potential side terminal of the power source and is non-active continuously in the addressing. The timing signal TSC repeats on and off at the row selection period in the addressing, so as to prevent the power source from a short circuit. The timing signal TSC' is a control signal unique to the present invention and is a timing signal TSC that passed through the delay circuit 81. The output circuit 131 changes the connection state of the data electrodes A_1-A_M with the power source circuit 41 in accordance with the switching signal from the output control circuit 121.

As shown in Fig. 5, the above-mentioned output control circuit 121 is a set of logic circuits 201, each of which is provided for each of the data electrodes A_1-A_M. In addition, the output circuit 131 is also a set of switching circuits 301, each of which is provided for each of the data electrodes A_1-A_M.

The logic circuit 201, which includes a plurality of gate circuits 211-216, outputs switching signals UP and DOWN having logical levels indicated by a truth table in Fig. 5. The switching circuit 301 comprises a pair of field effect transistors (hereinafter referred to as transistors) Q1 and Q2 connected serially as a switching element between the power source terminals, and protection diodes D1 and D2 connected between the source and the drain of the transistors Q1 and Q2 in the opposite direction. The transistor Q1 of the current supply terminal side of the power source is controlled by the switching signal UP, while the transistor Q2 of the current sink terminal side is controlled by the switching signal DOWN.

As shown in Fig. 6, in the FET (field effect transistor), a backward current path, which includes a parasitic diode d_0 and a parasitic resister r_0, is formed in parallel with the closed circuit including the switch SW and an inner resister R_0. Therefore, even if the diodes D1 and D2 are omitted in the switching circuit 301, the parasitic diode d_0 can be used for realizing the L reset and the H reset. However, characteristics of the parasitic diode d_0 may vary and can be defective, so it is desirable to provide the diodes D1 and D2 adding to the

parasitic diode d_0.

As shown in Fig. 7, in a first embodiment, the timing signal TSC is delayed so that the on and off timings of the switching signal UP are shifted from that of the switching signal DOWN for the row selection period Ty. In other words, the switching signal DOWN corresponds to the timing signal TSC, while the switching signal UP corresponds to the timing signal TSC' that is delayed from the timing signal TSC by the time t. By this timing setting, only the switching signal DOWN is turned on at the boundary of the row selection and the L reset is realized in the case where the change of the display data D_m and D_{m+1} given to the neighboring data electrodes A_m and A_{m+1} are opposite to each other as shown in Fig. 8. The time t (the delay time of the delay circuit 81) is selected in accordance with the time constant of the discharge current path connecting the neighboring data electrodes to each other in the L reset, so as to be longer than the time necessary for discharging the charge stored in the capacitance between the neighboring data electrodes.

In the delay by an RC circuit shown in Fig. 9A and an LC circuit shown in Fig. 9B, the signal is delayed by the time constant determined by the circuit constant. It is possible to delay the signal by the time corresponding to the sum of the delay time of the buffer circuits that are connected in series. In the delay by the shift register, the delay time can be adjusted by setting the frequency of the clock given to a flip-flop.

As shown in Fig. 10, the L reset can be also

realized by providing a delay circuit 81b for each of the data electrodes A_1-A_M instead of delaying the timing signal TSC. The switching signal DOWN is given directly to the transistor Q2 of the switching circuit 301 from the logic circuit 201b generating the signal corresponding to the combination of the timing signal TSC and the display data D_m, while the switching signal UP is given to the transistor Q1 via the delay circuit 81b.

Fig. 11 shows only the elements related to the data electrode and control thereof.

In a second embodiment, the timing signal TSC is delayed so that the on and off timings of the switching signals UP and DOWN are different between an odd column and an even column.

The display device 2 comprises a display panel 12 and a drive unit 22. The drive unit 22 includes a controller 32, a power source circuit 42, a driver 62A for odd column data electrodes, a driver 62B for even column data electrodes and a delay circuit 82. The driver 62A comprises a plurality of integrated circuit chips 72_1-72_k, while the driver 62B comprises a plurality of integrated circuit chips 72_{k+1}-72_{2k}. The structure in which the drivers of the data electrode are disposed at both sides in the column direction is suitable for the case where the column pitch is small. The controller 32 transfers the display data D_{odd} of odd columns to the driver 62A serially and transfers the display data D_{even} of even columns to the driver 62B serially every row selection period Ty in the addressing. The control signals LAT and SUS are given to the drivers 62A and 62B commonly. The

timing signal TSC is given only to the driver 62A, while the signal TSC', which is delayed from the timing signal TSC, is given to the driver 62B.

By this circuit structure, the L reset in which only the switching signal DOWN is turned on at the boundary of the row selections or the H reset in which only the switching signal UP is turned on can be realized when the change of the display data D_m and D_{m+1} are opposite between the neighboring data electrodes A_m and A_{m+1} as shown in Fig. 12.

According to the first embodiment and the second embodiment mentioned above, the integrated circuit chips, which were used conventionally, can be used for constituting the driver. In addition, the delay time of the signal can be adjusted, so as to support various display panels having different capacitance between the data electrodes. Therefore, the drive unit can be used for various display panels.

As shown in Fig. 13, in a third embodiment, display data of an even column are delayed from that of an odd column, so that the on and off timings of the switching signals UP and DOWN are different between the odd column and the even column.

The display device 3 includes a display panel 13, a controller 33 and a driver 63 being in charge of controlling all data electrodes A_1-A_M. The driver 63 comprises a shift register 103, a latch circuit 113, an output control circuit 123 and an output circuit 143. The output circuit 143 is a set of circuits that are similar to the switching circuit 301 shown in Fig. 10, while the

output control circuit 123 is a set of circuits that are similar to the logic circuit 201b shown in Fig. 10. In the display device 3, the latch circuit 113 is structured to latch by one step for odd columns and by two steps for even columns. By this structure, the second step of latch is delayed, so that the on and off timings of the switching signals UP and DOWN are shifted for realizing the L reset and the H reset. Furthermore, it is possible to structure the on and off control of the delay can be performed, so that the switching control related to the L reset and the H reset is performed only for a specific display pattern.

As shown in Fig. 14, in a fourth embodiment, the control signal LAT is delayed so that the on and off timings of the switching signals UP and DOWN are different between an odd column and an even column.

The display device 4 comprises a display panel 14 and a drive unit 24. The drive unit 24 includes a controller 34, a power source circuit 44, a driver 64A of data electrodes of odd columns, a driver 64B of data electrodes of even columns and a delay circuit 84. The driver 64A comprises a plurality of integrated circuit chips 74_1-74_k, while the driver 64B comprises a plurality of integrated circuit chips 74_{k+1}-74_{2k}. The controller 34 transfers display data D_{odd} of odd columns to the driver 64A serially and transfers display data D_{even} of even columns to the driver 64B serially every row selection period Ty in addressing. The control signals SUS and TSC to the drivers 64A and 64B commonly. The control signal LAT is given only to the driver 64A, while the signal TSC'

that is delayed from the control signal LAT is given to the driver 64B.

As shown in Fig. 15, in a fifth embodiment, a driver having delay means is used for delaying display data of an odd column from display data of an even column, so that the on and off timings of the switching signals UP and DOWN are different between the odd column and the even column.

The display device 5 comprises a display panel 15 and a drive unit 25. The drive unit 25 includes a controller 35, a power source circuit 45, a driver 65A of data electrodes of odd columns and a driver 65B of data electrodes of even columns. The controller 35 transfers the display data D_{odd} of the odd columns to the driver 65A serially and transfers the display data D_{even} of the even columns to the driver 65B serially every row selection period Ty in the addressing. The control signals LAT, SUS and TSC are given to the drivers 65A and 65B commonly. The control signal LAT is given only to the driver 64A, while a signal TSC' delayed from the control signal LAT is given to the driver 64B.

The driver 65A includes a two-step latch circuit 115A for latching display data D_{odd} of odd columns outputted by a shift register (not shown) in parallel. The driver 65B includes a one-step latch circuit 115B for latching display data D_{even} of even columns outputted by a shift register (not shown) in parallel. Since the latch circuit 115A is different from the latch circuit 115B about the step number, the on and off timings of the switching signals UP and DOWN are different between the

odd column and the even column. Each of the drivers 65A and 65B comprises a plurality of integrated circuit chips.

According to the fifth embodiment, an integrated circuit chip having delay function for constituting the driver 65A can be used as mixed with the conventional integrated circuit chip having no delay function for constituting the driver 65B, so that the stocked conventional components are also used for realizing the present invention without waste.

INDUSTRIAL AVAILABILITY

As explained above, undesired power consumption due to capacitance between data electrodes in a display panel can be reduced by applying the present invention.